A Spline Large-Signal FET Model Based on Bias-Dependent Pulsed *I–V* Measurement

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***Abstract*—A spline large-signal FET model is presented. This includes a quiescent bias dependency to predict nonlinear dynamic behavior of FETs in which self-heating and trap effects are present. The intrinsic device of the model represented by a parallel connection of current and charge sources and the model parameters are extracted from bias-dependent pulsed *I–V*s and S-parameters, respectively. The validity of the model is demonstrated by comparing the simulated small-signal S-parameters over a wide bias range with measured data. Nonlinear behaviors of FETs such as $P_{\rm in} - P_{\rm out}$, third-order intermodulation distortion, and efficiency are also compared.**

***Index Terms*—GaAs MESFET, large-signal model, nonquasi-static model, pulsed I–V, self-heating effects, spline, table-based model, trap effects.**

I. Introduction

ACCURATE large-signal FET models are absolutely necessary for computer-aided high-frequency circuit design, especially for power-amplifier design. Large-signal device models have evolved into three basic types, i.e., physical, empirical, and table-based models. Although analytic empirical models are widely used because of their simplicity, they require good model formulation and an optimization process during their model parameter extraction in order to fit measured data with reasonable accuracy. Moreover, nonphysical parameters are typically added to attain accuracy in a wide range of operation voltages, and the models still fall short in accuracy because of their imposed rigid analytic expressions. An alternative approach is a table-based model, which stores extracted model parameters at many bias points directly in a table. Table-based models have demonstrated their abilities to accurately predict device performances, and these models are technology independent [1]–[4]. They also eliminate the need of optimization in the model-extraction process. These make the model versatile and efficient. A problem associated with table-based model is the existence of discontinuities in model elements or their first derivatives. In spline model, the property of the B spline preserves monotonicity and convexity because a function constructed from the B spline of polynomial degree k can be made continuous to the $(k-1)$th derivative. This is the very reason to use the spline model.

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Several groups have suggested simplified nonquasi-static approaches to improve the accuracy of FET models at high frequency [1]–[3]. Daniels *et al.* represented the total current of each MESFET's node as a sum of conduction current and displacement current that can be obtained simply by path integration of small-signal conductances and capacitances [1]. Roques *et al.* modeled the intrinsic region of a pseudomorphic high electron-mobility transistor (p-HEMT) as a distributed R–C–g_m network and calculated each node current using an integration of small-signal expression similar to that of Daniels *et al.* [2]. In these two cases, it is required for the model parameters to satisfy integration path-independence rules in order to obtain charges and RF currents from the measured small-signal responses. However, the path independence is only valid for small nondispersive devices in which self-heating and trap effects are not important. Wei *et al.* suggested a specific integration path considering self-heating effects [3]. However, they omitted trap effects and assumed that the major dispersion effect is self-heating. The model described in this paper includes both self-heating and trap effects. The model parameters for self-heating and trap effects are obtained from bias-dependent pulsed *I–V*s, which allow the characterizations under isothermal and isotrap conditions.

II. Model Description

A large-signal FET model assumes that the intrinsic device nonlinearities can be represented by a parallel connection of voltage-controlled current sources and charge-based nonlinear capacitors [1], [2], [4]. The large-signal equivalent circuit, shown in Fig. 1, uses three charge sources ($Q_{0,g}, Q_{0,d}, Q_{0,s}$), three current sources ($I_{0,g}, I_{0,d}, I_{0,s}$), and eight R–L–C extrinsic elements.

The extrinsic elements are extracted by using a cold FET measurement approach [5]–[7], and the intrinsic elements are directly calculated from the pulsed *I–V*s and measured S-parameters at various bias points.

The total current into node k (gate or drain at common source configuration) is the sum of conduction currents $(I_{\rm cond})$ from current sources and displacement currents $(I_{\rm disp})$ from charge sources as follows:

$$I_k(t) = I_{{\rm cond},k}(t) + I_{{\rm disp},k}(t) \tag{1}$$

The conduction current at the gate node $(I_{0,g})$ modeled as a parallel connection of two Schottky diodes can be described as

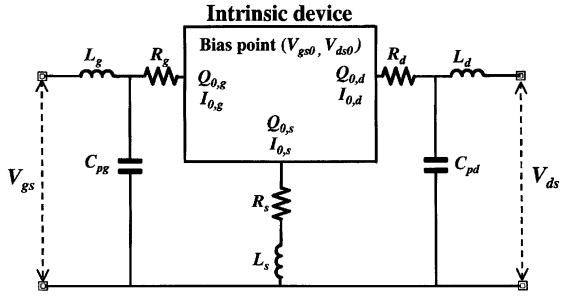


Fig. 1. Schematic of the MESFET model.

follows:

$$I_{0,g}(v_{\rm gs}, v_{\rm ds}) = I_{s1}\left\{\exp\left(\frac{v_{\rm gs}}{V_t}\right) - 1\right\} + I_{s2}\left\{\exp\left(\frac{v_{\rm gs} - v_{\rm ds}}{V_t}\right) - 1\right\} \quad (2)$$

where I_{s1}, I_{s2} and V_t are fitting parameters and can be obtained from *I–V* measurements. The conduction current at the drain node (I_0, d) is the main nonlinear component in FET models. The presence of self-heating and trap effects in FET devices causes great difficulty in modeling $I_{0,d}$. The self-heating and trap effects are varied by quiescent bias $(V_{\rm gs0}, V_{\rm ds0})$ [8]–[12]. Thus, $I_{0,d}$ must be included in the dependence on quiescent bias. If it is assumed that the self-heating and trap effects modify the channel current in a multiplicative way, $I_{0,d}$ can be expressed as [8], [9]

$$I_{0,d}(v_{\rm gs}, v_{\rm ds}, V_{\rm gs0}, V_{\rm ds0}) = I_{\rm ds0}(v_{\rm gs}, v_{\rm ds}) \times f_{\rm trap} \times f_{\rm thermal} \quad (3)$$

where $I_{\rm ds0}$ is pulsed *I–V* at the zero quiescent bias ($V_{\rm gs0} = 0$ V, $V_{\rm ds0} = 0$ V). $I_{\rm ds0}$ serves as a reference to describe self-heating and trap effects, which means that $f_{\rm trap}$ and $f_{\rm thermal}$ become unity at the bias condition as follows:

$$f_{\rm trap}|_{V_{\rm gs0}=0, V_{\rm ds0}=0} = 1 \quad f_{\rm themal}|_{V_{\rm gs0}=0, V_{\rm ds0}=0} = 1. \quad (4)$$

In case $V_{\rm gs0}$ is lower than the threshold voltage $(V_{\rm th})$, $f_{\rm thermal}$ becomes unity due to negligible power dissipation as follows:

$$f_{\rm themal}|_{V_{\rm gs0} < V_{\rm th}} = 1. \quad (5)$$

$I_{\rm ds0}$ is fitted using B-spline functions with fifth-order [13]. $f_{\rm trap}$ and $f_{\rm thermal}$ are obtained from pulsed *I–V*s of multiple biases. $f_{\rm trap}$ is used here to account for the channel current variation due to the trap effects. Electrons captured in traps at the quiescent bias affect the channel current because they remain in traps after the pulse is applied when the pulsewidth is shorter than the emission time constant (a few milliseconds) [10]. There are two types of traps in the MESFET, i.e., the bulk and surface state traps. The effects of the bulk trap depends on the quiescent drain bias, and are related to the reduction of the channel current. To the contrast, the effects of the surface state trap depends on both the quiescent drain and gate biases, and are related to the increase of the breakdown voltage [11]. Since the bulk-trap effects are dominant below the breakdown region, the effect of $V_{\rm gs0}$ can be negligible and $f_{\rm trap}$ can be expressed as

$$f_{\rm trap} = f(V_{\rm ds0}, v_{\rm gs}, v_{\rm ds}). \quad (6)$$

Since $f_{\rm trap}$ becomes unity at zero quiescent drain bias, from (3)–(6), $f_{\rm trap}$ can be obtained using

$$f_{\rm trap}(V_{\rm ds0}, v_{\rm gs}, v_{\rm ds}) = \frac{I_{\rm ds}(V_{\rm th}, V_{\rm ds0}, v_{\rm gs}, v_{\rm ds})}{I_{\rm ds}(V_{\rm th}, V_{\rm ds0} = 0, v_{\rm gs}, v_{\rm ds})} \quad (7)$$

where $I_{\rm ds}$ represents the pulsed *I–V* at the quiescent bias $V_{\rm gs0}$ and $V_{\rm ds0}$. In our model, the extracted values of $f_{\rm trap}$ are fitted using a fifth-order B-spline function whose value is determined by $V_{\rm ds0}, v_{\rm gs}$ and $v_{\rm ds}$.

$f_{\rm thermal}$ is used here to account for the channel current variation with the temperature increase due to internal power dissipation $(P_{\rm diss})$, and it can be expressed as a function of only $P_{\rm diss}$ as follows:

$$f_{\rm thermal} = f(P_{\rm diss}), \qquad \text{where } P_{\rm diss} = V_{\rm ds0} \cdot I_{\rm ds}^{\rm DC}(V_{\rm gs0}, V_{\rm ds0}) \quad (8)$$

where $I_{\rm ds}^{\rm DC}$ describes the dc *I–V*. The electrical power dissipated in the channel of the device is the principal cause of changes to the electron mobility (μ_n), which, in turn, reduce the channel current mainly due to degradation in the scatter-limited electron drift velocity. Thus, $f_{\rm thermal}$ is related with electron mobility. Since there exists a linear relationship between $\log(\mu_n)$ and $\log(T)$ [14], and the channel temperature (T) is proportional to the power dissipation $(P_{\rm diss})$, $f_{\rm thermal}$ can be modeled as

$$\log(f_{\rm thermal}) = a + b \times \log(P_{\rm diss}) \quad (9)$$

where a and b are fitting parameters.

From (3), (5), (6), and (8), $f_{\rm thermal}$ can be obtained using

$$f_{\rm thermal}\Big(P_{\rm diss}(V_{\rm gs0}, V_{\rm ds0})\Big) = \frac{I_{\rm ds}(V_{\rm gs0}, V_{\rm ds0}, v_{\rm gs}, v_{\rm ds})}{I_{\rm ds}(V_{\rm th}, V_{\rm ds0}, v_{\rm gs}, v_{\rm ds})}. \quad (10)$$

The extracted values of $f_{\rm thermal}$ are used to obtain thermal model parameter a and b in (9).

Current conservation gives the equation of $I_{0,s}$ as follows:

$$I_{0,s} = -(I_{0,g} + I_{0,d}). \quad (11)$$

If a relaxation time approximation can be assumed, the displacement current at a given node k can be described [1] as follows:

$$I_{{\rm disp},k}(t) = \frac{dQ_{0,k}(V_{\rm gs}, V_{\rm ds})}{dt} - \frac{d}{dt}\Big(\tau_k(V_{\rm gs}, V_{\rm ds}) I_{{\rm disp},k}(t)\Big) \quad (12)$$

where $Q_{0,k}$ is the quasi-static charge at node k and τ_k is the charge redistribution time constant, which is used to represent

nonquasi-static effects at high frequency. It has been verified that the integration of charge terms is approximately path independent [1]–[4]. Thus, we perform integration of small-signal conductances with respect to port voltages to obtain $Q_{0,k}$. The relation between the large-signal model elements and the small-signal parameters is derived by rewriting (1) with (12), then linearizing with respect to gate–source and drain–source voltages as follows:

$$i_k = \frac{\partial I_{0,k}}{\partial V_{\rm gs}} v_{\rm gs} + \frac{\partial I_{0,k}}{\partial V_{\rm ds}} v_{\rm ds} + \frac{j\omega}{1+j\omega\tau_{kg}} \cdot \frac{\partial Q_{0,k}}{\partial V_{\rm gs}} v_{\rm gs} + \frac{j\omega}{1+j\omega\tau_{kd}} \cdot \frac{\partial Q_{0,k}}{\partial V_{\rm ds}} v_{\rm ds} \quad (13)$$

where $j=\sqrt{-1}, \omega = 2\pi f, i_k$ is the small-signal current at the k node. The partial derivatives of the model element $I_{0,k}$ and $Q_{0,k}$ and delay element τ_{kl} can be described simply in terms of the intrinsic Y-parameters by applying (13) to the gate and drain nodes and using the definition of the common-source Y-parameters as follows:

$$Y_{kl} = \frac{i_k}{v_l} = g_{kl} + \frac{j\omega c_{kl}}{1+j\omega\tau_{kl}} \approx g_{kl} + \omega^2 c_{kl}\tau_{kl} + j\omega c_{kl} \quad (14)$$

where g_{kl} is the partial derivative of $I_{0,k}$, and c_{kl} is the partial derivative of $Q_{0,k}$. This equation is similar to the small-signal model equations of [1] and [2]. g_{kl}, c_{kl}, and τ_{kl} are functions of bias points and can be determined by fitting the expressions on the right-hand side of (14) to each of the four intrinsic Y-parameters at various bias points. The obtained g_{kl} is not used to get $I_{0,d}$ because bias-dependent S-parameters are not adequate to model the self-heating and trap effects and $I_{0,d}$ is obtained directly from bias-dependent pulsed *I–V*s. For small-signal simulation, g_{21} and g_{22} are calculated from differentiating (3) with respect to $v_{\rm gs}$ and $v_{\rm ds}$, respectively. Since g_{21} and g_{22} are intrinsic components and $v_{\rm gs}$ and $v_{\rm ds}$ are external port voltages, voltage drop by parasitic resistors must be considered as follows:

$$g_{21} = \frac{g_m}{1-g_m \cdot R_s}, \qquad \text{where } g_m = \partial I_{0,d}/\partial v_{\rm gs} \quad (15)$$

$$g_{22} = \frac{g_{\rm ds}}{1-g_{\rm ds}\cdot(R_s+R_d)}, \qquad \text{where } g_{\rm ds} = \partial I_{0,d}/\partial v_{\rm ds}. \quad (16)$$

The obtained $c_{\rm kl}$ and τ_{kl} are modeled using B-spline functions with fifth order. $Q_{0,k}$ can be obtained easily by path integration of c_{kl} and an integration of the spline function is represented by very simple analytic form [13]. Charge conservation gives the equation of $Q_{0,s}$ as follows:

$$Q_{0,s} = -\big(Q_{0,g} + Q_{0,d}\big). \quad (17)$$

III. Model Extraction and Implementation

To demonstrate the model, we extracted model elements of a $2 \times 0.6 \times 50$ μm^2 GaAs MESFET. The device has a threshold voltage of -0.6 V and a peak unity current gain cutoff frequency of 18 GHz.

TABLE I
Extracted Value of Parasitic Elements

R_g = 0.95 Ω	R_d = 2.92 Ω	R_s = 2.13 Ω
L_g = 21.07 pH	L_d = 20.71 pH	L_s = 0 pH
C_{pg} = 0.11 pF	C_{pd} = 0.27 pF	

Prior to extracting model elements, parasitic elements associated with the metal pad structure and the contact resistances are deembedded from the measured data to provide intrinsic small-signal parameters. Parasitic elements that are deembedded from the data include series resistors (R_g, R_d, R_s) and inductors (L_g, L_d, L_s) and pad capacitances (C_{pg}, C_{pd}). All parasitic elements are assumed independent of bias. Cold FET measurements are performed at 17 bias points covering the range $V_{\rm gs0} = 0$ to 0.8 V. The series resistors and inductors are calculated with a standard procedure using forward gate-bias S-parameters under a cold FET condition [5], [6], and the pad capacitances are calculated using pinched-off gate bias S-parameters under a cold FET condition [7]. Extracted values are given in Table I.

The resulting intrinsic Y-parameters are used to determine g_{kl}, c_{kl}, and τ_{kl} at each bias point using the relation in (14). S-parameters were measured at 465 bias points covering the range $V_{\rm gs0} = -0.8$ to 0.6 V, $V_{\rm ds0} = 0$ to 6 V, with the frequency range from 0.5 to 18 GHz. The extracted bias-dependent c_{kl} and τ_{kl} are used for getting fifth-order B-spline coefficients, which are needed to generate interpolated values using the B-spline function. An equation for the general spline function is as follows [13]:

$$S\big(V_{\rm gs0}, V_{\rm ds0}\big) = \sum_{j=1}^{N_2}\sum_{i=1}^{N_1} \alpha_{i,j} B_i\big(V_{\rm gs0}, P_1\big) B_j\big(V_{\rm ds0}, P_2\big) \quad (18)$$

where S is the spline function, $\alpha_{i,j}$ is the spline coefficient, and B_i, B_j are one-dimensional B-spline bases, P_1 and P_2 are a set of spline knot points in the $V_{\rm gs0}$ and $V_{\rm ds0}$ plane, and N_1 and N_2 represent the number of one-dimensional B-spline coefficients.

Pulsed *I–V*s for the self-heating effects modeling are measured at 24 different bias points covering the range $V_{\rm gs}0 = -0.6$ to 0.6 V, $V_{\rm ds0} = 0$ to 6 V. All pulsed *I–V* data were obtained by setting the pulsewidth to 400 ns and the period to 100 μs. The measurements during such a short time ensure that the device temperature is kept constant [10]. Fig. 2 shows the pulsed *I–V* data measured as the gate quiescent bias was changed ($V_{\rm gs0} = -0.6, -0.4, -0.2, 0.0, 0.2, 0.6$ V) with the fixed drain quiescent voltage ($V_{\rm ds0} = 6$ V). Fig. 3 shows the modeled and measured $f_{\rm thermal}$. We can deembed the self-heating effects by dividing the pulsed *I–V* data by $f_{\rm thermal}$. All resultant data became overlapped to the one measured at the threshold voltage of -0.6 V, as shown in Fig. 4. This shows that the self-heating effects have been successfully deembedded and the thermal model is valid.

Pulsed *I–V*s for the trap effects modeling were also measured at 31 bias points covering the range $V_{\rm ds0} = 0$ to 6 V, while $V_{\rm gs0}$ was fixed at -0.6 V, which was sufficiently low to eliminate the self-heating effects. These are shown in Fig. 5. Extracted

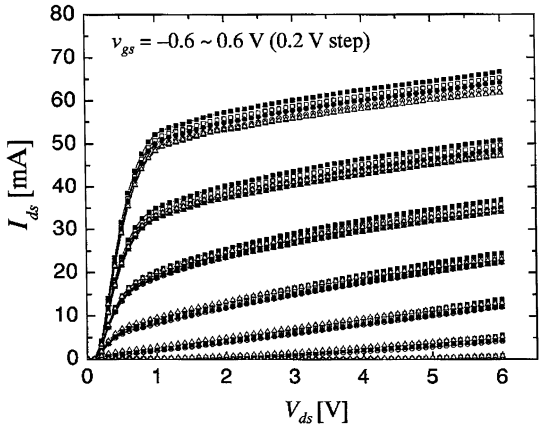


Fig. 2. Pulsed *I–V* measured as the gate quiescent bias was swept while the drain quiescent bias was fixed. $V_{\rm gs0} = -0.6\,(\blacksquare), -0.4\,(\square), -0.2\,(\bullet), 0.0\,(\bigcirc), 0.2\,(\blacktriangle), 0.6\,(\triangle)$ V at $V_{\rm ds0} = 6$ V.

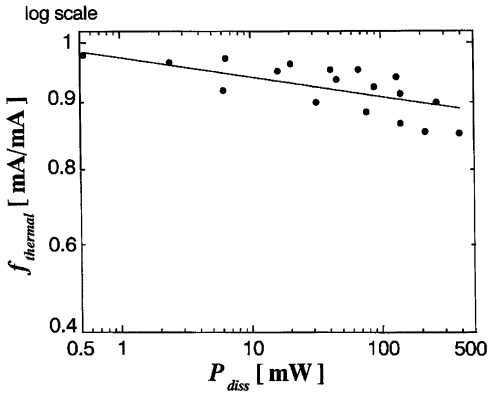


Fig. 3. Comparison of the measured (dots) and modeled (solid line) $f_{\rm thermal}$.

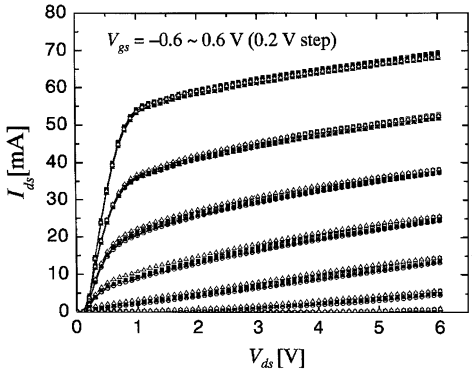


Fig. 4. After deembedding self-heating effects. $V_{\rm gs0} = -0.6\,(\blacksquare), -0.4\,(\square), -0.2\,(\bullet), 0.0\,(\bigcirc), 0.2\,(\blacktriangle), 0.6\,(\triangle)$ V at $V_{\rm ds0} = 6$ V.

values of $f_{\rm trap}$ using (7) were used to get coefficients for a three-dimensional (3-D) spline function whose value is determined by $V_{\rm ds0}, v_{\rm gs}$ and $v_{\rm ds}$. Fig. 6 shows the pulsed *I–V* data, which are divided by $f_{\rm trap}$. As a result, all pulsed *I–V* data measured from four different $V_{\rm ds0}$'s become overlapped. It is apparent that the trap effects have been successfully deembedded and the trap model is valid.

Circuit analysis is performed using HP ADS and our model was installed in HP ADS using a user-defined model, which is

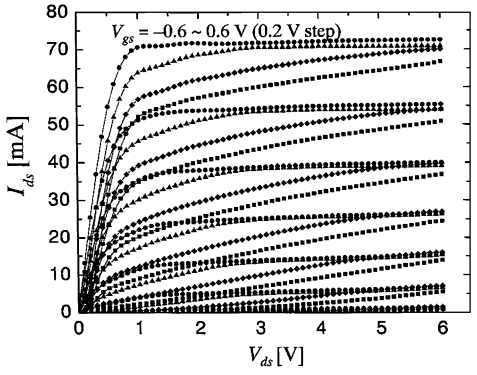


Fig. 5. Pulsed *I–V* measured as the drain quiescent bias was swept while the gate quiescent bias was fixed. $V_{\rm ds0} = 0\,(\bullet), 2\,(\blacktriangle), 4\,(\diamond), 6\,(\blacksquare)$ V at $V_{\rm gs0} = -0.6$ V.

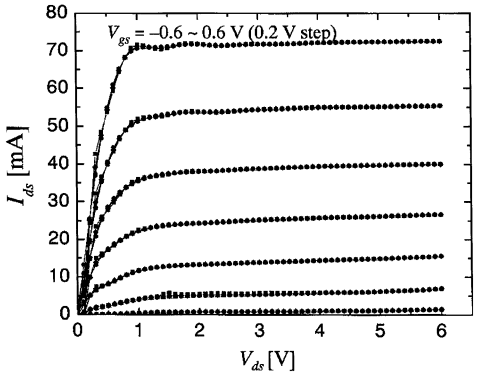


Fig. 6. After deembedding trap effects. $V_{\rm ds0} = 0\,(\bullet), 2\,(\blacktriangle), 4\,(\diamond), 6\,(\blacksquare)$ V at $V_{\rm gs0} = -0.6$ V.

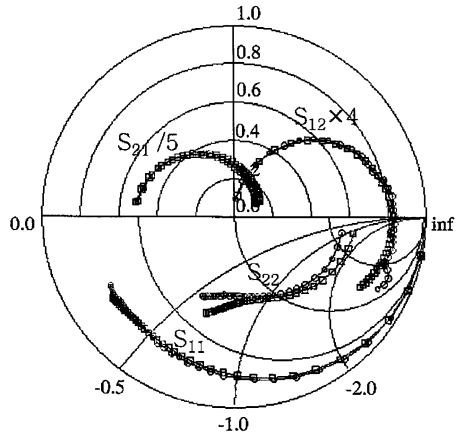
offered to install specific C-coded models. Once the quasi-static currents, charges, and delays are determined, the model can be implemented for a large-signal harmonic-balance mode, as well as for a small-signal ac mode.

IV. Model Validation

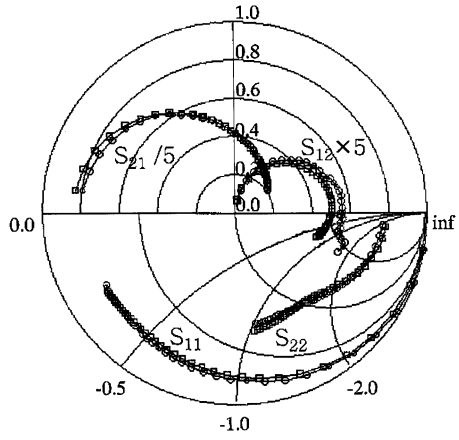
Small-signal simulations with the large-signal model were performed at 465 bias points covering the range $V_{\rm gs0} = -0.8$ to 0.6 V, $V_{\rm ds0} = 0$ to 6 V, with a frequency range from 0.5 to 18 GHz, and compared to the measured S-parameters. Fig. 7(a) and (b) shows the simulated and measured S-parameters close to the linear region ($V_{\rm ds0} = 0.6$ V, $V_{\rm gs0} = -0.2$) and in the saturation region ($V_{\rm ds0} = 4$ V, $V_{\rm gs0} = -0.2$), respectively. The agreement between the modeled and measured data is very good. Fig. 8 shows errors of S-parameters between the modeled and measured data at various bias points. The error is defined by

$$E = \frac{1}{4N}\sum_{i=1}^{N}\left[\left(\frac{S_{11}^{\rm mea} - S_{11}^{\rm mod}}{S_{11}^{\rm mea}}\right)^2 + \left(\frac{S_{12}^{\rm mea} - S_{12}^{\rm mod}}{S_{12}^{\rm mea}}\right)^2 + \left(S_{21}^{\rm mea} - S_{21}^{\rm mod}\right)^2 + \left(\frac{S_{22}^{\rm mea} - S_{22}^{\rm mod}}{S_{22}^{\rm mea}}\right)^2\right] \tag{19}$$

where N is the number of frequency points. The errors do not exceed 3%. This also validates that the proposed large-signal



(a)



(b)

Fig. 7. Small-signal S-parameters. Simulation versus measurement. (a) At $V_{\rm gs0} = -0.2$ V and $V_{\rm ds0} = 0.6$ V. (b) At $V_{\rm gs0} = -0.2$ V and $V_{\rm ds0} = 4$ V. □: simulation. ○: measurement.

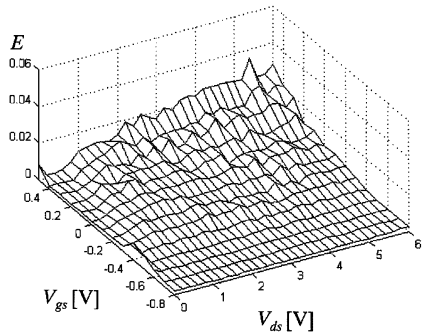


Fig. 8. Errors between the measured and simulated S-parameters.

model is accurate in reproducing the small-signal characteristics.

The simulated dc *I–V* characteristics of the MESFET over the voltage range $V_{\rm gs0} = -0.8$ to 0.6 V, $V_{\rm ds0} = 0$ to 6 V are shown in Fig. 9. During this simulation, $V_{\rm gs0}$ and $V_{\rm ds0}$ follow $v_{\rm gs}$ and $v_{\rm ds}$, respectively, in (3). High-frequency *I–V* characteristics of the MESFET at various quiescent bias points are also simulated and compared with pulsed *I–V*s. High-frequency *I–V*s are simulated using (3) under the fixed $V_{\rm gs0}$ and $V_{\rm ds0}$ condition. Fig. 10 shows the simulated and measured high-frequency *I–V* characteristics at an arbitrary quiescent bias ($V_{\rm ds0} = 4$ V, $V_{\rm gs0} = -0.2$). Good agreements between simulated and measured results show that the model is accurate in both dc and high-frequency simulation.

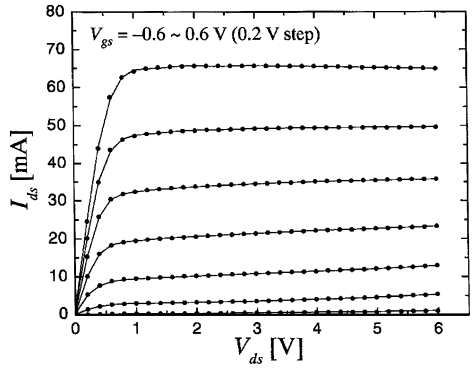


Fig. 9. DC *I–V* characteristics. Simulation (solid lines) versus measurement (dots).

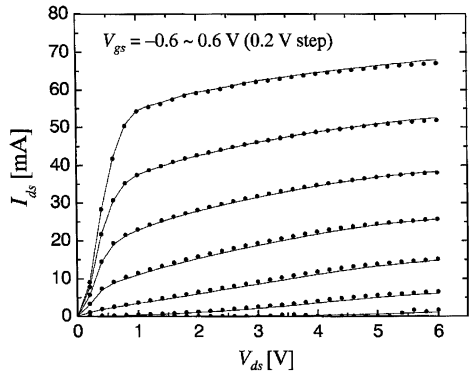


Fig. 10. High-frequency *I–V* characteristics. Simulation (solid lines) versus measurement (dots) at $V_{\rm gs0} = -0.2$ V and $V_{\rm ds0} = 4$ V.

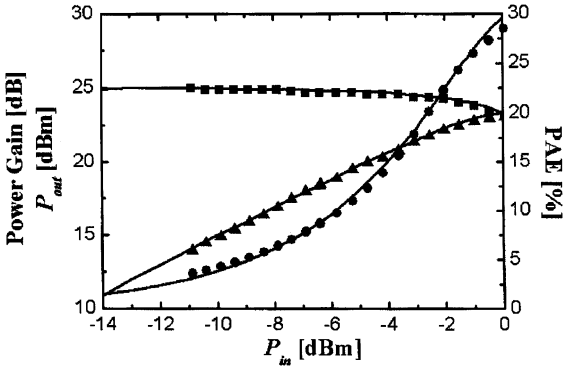


Fig. 11. Simulated and measured one-tone test at 1.95 GHz. Measurement: ■ ($G_{\rm power}$), ▲ ($P_{\rm out}$), • (PAE). Simulation: line.

To verify large-signal characteristics, we also extracted model parameters of a packaged GaAs MESFET, which has a saturation current ($I_{\rm dss}$) of 200 mA and a drain–source breakdown voltage of 20 V. A one- and two-tone test were performed at a bias condition ($V_{\rm ds} = 10$ V, $I_{\rm ds} = 80$ mA) and a matching condition ($\Gamma_{\rm source} = 0.825\angle 119.6°, \Gamma_{\rm load} = 0.734\angle 74.3°$).

Fig. 11 shows the simulated and measured one-tone test. Simulation results perfectly predict power gain, output power, and

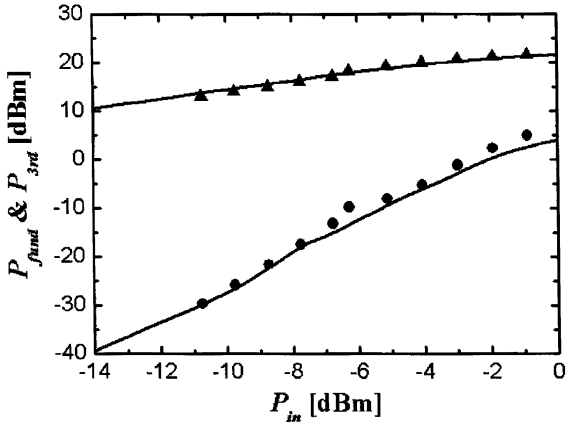


Fig. 12. Simulated and measure two-tone test at 1.95 GHz. Measurement: ■ $(P_{\rm fund})$, ▲ $(P_{\rm 3rd})$. Simulation: line.

power-added efficiency (PAE). Comparison between simulated and measured third-order intermodulation (IM3) is shown in Fig. 12. This figure shows the model is very accurate in reproducing the nonlinear characteristics of FETs.

V. Conclusion

A nonlinear FET model with thermal and trap effects has been introduced and the extraction method of the model parameters has also been presented. The model parameters can be extracted using pulsed *I–V*s and S-parameters, which are measured as the quiescent voltages are changed. The model shows an excellent agreement between measured and simulated data in both small- and large-signal characteristics.

References

[1] R. R. Daniels, A. T. Yang, and J. P. Harrang, "A universal large/small signal 3-terminal FET model using a nonquasi-static charge-based approach," *IEEE Trans. Electron Devices*, vol. 40, pp. 1723–1729, Oct. 1993.

[2] D. Roques, F. Brasseau, B. Cogo, M. Soulard, and J.-L. Cazaux, "A non quasistatic nonlinear p-HEMT model operating up to millimetric frequencies," *Electron. Lett.*, vol. 36, no. 10, pp. 857–858, May 2000.

[3] C.-J. Wei, A. Tkachenko, and D. Bartle, "Table-based dynamic FET model assembled from small-signal models," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 700–705, June 1999.

[4] D. E. Root and S. Fan, "Experimental evaluation large-signal modeling assumptions based on vector analysis of bias-dependent S-parameter from MESFET's and HEMTs," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, 1992, pp. 255–258.

[5] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1151–1159, July 1988.

[6] M. Berroth and R. Bosch, "High-frequency equivalent circuit of GaAs FET's for large-signal applications," *IEEE Trans. Microwave Theory Tech.*, vol. 39, pp. 224–229, Feb. 1991.

[7] P. M. White and R. M. Healy, "Improved equivalent circuit for determination of MESFET and HEMT parasitic capacitances from cold FET measurements," *IEEE Microwave Guided Wave Lett.*, vol. 3, pp. 453–454, Dec. 1993.

[8] A. K. Jastrzebski, "Characterization and modeling of temperature and dispersion effects in power MESFETs," in *24th Eur. Microwave Conf.*, 1994, pp. 1319–1324.

[9] P. H. Ladbrooke, A. K. Jastrzebski, R. J. Donarski, J. P. Bridge, and J. E. Barnaby, "Mechanism of drain current droop in GaAs MESFETs," *Electron. Lett.*, vol. 31, no. 21, pp. 1875–1876, Oct. 1995.

[10] Z. Ouarch, J. M. Collantes, J. P. Teyssier, and R. Quere, "Measurement based nonlinear electrothermal modeling of GaAs FET with dynamical trapping effects," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, 1998, pp. 599–602.

[11] T. M. Barton, C. M. Snowden, J. R. Richardson, and P. H. Ladbrooke, "Narrow pulse measurement of drain characteristics of GaAs MESFETs," *Electron. Lett.*, vol. 23, pp. 68–687, 1987.

[12] T. Fernandez, Y. Newport, J. M. Zamanillo, A. Tazon, and A. Mediavilla, "Extracting a bias-dependent large signal MESFET model from pulsed I/V measurements," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 372–378, Jan. 1996.

[13] C. de Boor, *A Practical Guide to Splines*. New York: Springer-Verlag, 1978.

[14] O. Madelung, *Data in Science and Technology: Semiconductors-Group IV Elements and III–V Compounds*. New York, NY: Springer-Verlag, 1991, p. 106.

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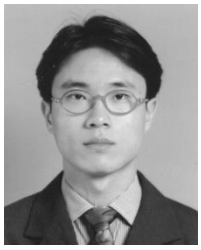

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